METHOD FOR ACHIEVING GLOBAL PLANARIZATION BY FORMING MINIMUM MESAS IN LARGE FIELD AREAS

This application is a continuation of application Ser. No. 08/633,620, filed Apr. 17, 1995, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor fabrication and more particularly to an improved process of globally planarizing a field dielectric by placing minimum mesas (hereinafter "silicon risers") in large area isolation regions.

2. Description of the Relevant Art

The fabrication of an integrated circuit involves placing numerous devices in a single semiconductor substrate. Select devices are interconnected by a conductor which extends over a dielectric which separates or "isolates" those devices. Implementing an electrical path across a monolithic integrated circuit thereby involves selectively connecting isolated devices. When fabricating integrated circuits it must therefore be possible to isolate devices built into the substrate from one another. From this perspective, isolation technology is one of the critical aspects of fabricating a functional integrated circuit.

A popular isolation technology used for an MOS integrated circuit involves the process of locally oxidizing silicon. Local oxidation of silicon, or LOCOS process involves oxidizing field regions between devices. The oxide grown in field regions are termed field oxide, wherein field oxide is grown during the initial stages of integrated circuit fabrication, before source and drain implants are placed in device areas or active areas. By growing a thick field oxide in isolation (or field) regions pre-implanted with a channel-stop dopant, LOCOS processing serves to prevent the establishment of parasitic channels in the field regions.

While LOCOS has remained a popular isolation technology, there are several problems inherent with LOCOS. First, a growing field oxide extends laterally as a bird's-beak structure. In many instances, the bird's-beak structure can unacceptably encroach into the device active area. Second, the pre-implanted channel-stop dopant oftentimes redistributes during the high temperatures associated with field oxide growth. Redistribution of channel-stop dopant primarily affects the active area periphery causing problems known as narrow-width effects. Third, the thickness of field oxide causes large elevational disparities across the semiconductor topography between field and active regions. Topological disparities cause planarity problems which become severe as circuit critical dimensions shrink. Lastly, thermal oxide growth is significantly thinner in small field (i.e., field areas of small lateral dimension) regions relative to large field regions. In small field regions, a phenomenon known as field-oxide-thinning effect therefore occurs. Field-oxide-thinning produces problems with respect to field threshold voltages, interconnect-to-substrate capacitance, and field-edge leakage in small field regions between closely spaced active areas.

Many of the problems associated with LOCOS technology are alleviated by an isolation technique known as the "shallow trench process". Despite advances made to decrease bird's-beak, channel-stop encroachment and nonplanarity, it appears that LOCOS technology is still inadequate for deep submicron MOS technologies. The shallow trench process is better suited for isolating densely spaced active devices having field regions less than one micron in lateral dimension.

The trench process involves the steps of etching a silicon substrate surface to a relatively shallow depth, e.g., between 0.2 to 0.5 microns, and then refilling the shallow trench with a deposited dielectric. Some trench processes include an interim step of growing oxide on trench walls prior to the trench being filled with a deposited dielectric. After the trench is filled, it is then planarized to complete the isolation structure.

The trench process eliminates bird's-beak and channel-stop dopant redistribution problems. In addition, the isolation structure is fully recessed, offering at least a potential for a planar surface. Still further, field-oxide thinning in narrow isolation spaces does not occur and the threshold voltage is constant as a function of channel width.

While the trench isolation process has many advantages over LOCOS, it cannot in all instances achieve complete global planarization across the entire semiconductor topography. The upper surface of fill dielectric in large isolation areas are generally at lower elevational levels than the upper surface fill dielectric in small isolation areas. The fill dielectric readily deposits in small area trenches such that the elevation of the fill dielectric in a small area is greater than the elevation within a large area trench. Accordingly, subsequent processing is needed to bring the large area fill topography to the same elevational level as small area fill topography.

Most researchers have focused upon fairly complex processes for planarizing large and small area fill dielectrics. Those processes generally involve rework of the fill dielectric. A popular rework technique involves depositing a sacrificial layer across the fill dielectric topography, and then removing the sacrificial layer at the same etch rate as the underlying dielectric. Generally, the sacrificial layer is deposited as a low-viscosity liquid. Baking the liquid, or exposing it to ultraviolet light, causes the liquid to convert to solid form, as a solid-gel reaction. Popular sacrificial materials include photoresist, polymide or spin-on glass (SOG). The sacrificial layers generally etch back in a plasma until the topmost regions of the fill dielectric are exposed. The etch chemistry is then modified so that the sacrificial layer material and the underlying fill dielectric are etched at approximately the same rate. The etch is continued until all of the sacrificial layer has been etched away, leaving a somewhat planar dielectric upper surface.

The sacrificial etchback technique is generally valid only for the planarization of topographies in which features are less than 10 μm (microns) apart. For large regions between trenches, the step height will not be reduced, since the photoresist thickness on top of such features will be the same as the thickness over the adjacent trench.

In an effort to overcome the shortcomings of the etchback process, a planarization block mask may be used. In this procedure, a liquid material is applied and developed as a planarization film followed by a block mask used to expose and develop this film. The block mask protects topography in wide, low regions from a subsequent etch plasma. The upper surface of high regions can then be removed to an elevational level commensurate with the protected low regions. The planarization block mask involves an additional lithography step and a mask which is produced by selectively reversing the mask used in producing the underlying topography. Mask reversal may involve errors due to changes in the resist thickness caused by the underlying pattern, misalignment, etc.

In an effort to eliminate the complex deposition, patterning and etch processes involved with sacrificial deposition,